

Amendments to the Claims

1. (Canceled).

2. (Canceled).

3. (Previously presented) The delay time adjusting circuit as claimed in claim 7, wherein said phase comparison circuit supplies a signal indicating said comparison result to said delay adjusting circuit according to said signal generated by said second divider and obtained via said dummy circuit.

4. (Canceled).

5. (Canceled).

6. (Canceled).

7. (Currently Amended) A delay time adjusting circuit for receiving a signal that is input to an input buffer, as an input signal for via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal, comprising:

a first divider configured to divide a frequency of said input signal by a first division rate;

a variable delay circuit, including a delay chain in which delay units are coupled in series, configured to delay said input signal by selecting a number of said delay units to output said output signal;

a second divider configured to divide a frequency of said output signal by a second division rate higher than said first division rate;

a dummy circuit configured to delay a signal from said second divider by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer;

a phase comparison circuit configured to compare phases of a signal from said first divider and a signal from said dummy circuit; and

a delay adjusting circuit configured to select the number of said delay units in response to a comparison result in said phase comparison circuit.

8. (Currently Amended) A delay time adjusting circuit for receiving a signal that is input buffer, as an input signal for via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal, comprising:

a variable delay circuit, including a delay chain in which delay units are coupled in series, configured to delay said input signal by selecting a number of said delay units to output said output signal;

a divider configured to divide a frequency of said output signal by a division rate, wherein a frequency of a signal from said divider is less than a frequency of said input signal;

a dummy circuit configured to delay a signal from said divider by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer;

a phase comparison circuit configured to compare phases of said input signal and said signal from said dummy circuit; and

a delay adjusting circuit configured to select the number of said delay units in response to a comparison result in said phase comparison circuit.

9. (Currently Amended) A delay time adjusting method for receiving a signal that is input to an input buffer, as an input signal via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal, comprising the steps of:

- (a) dividing a frequency of said input signal by a first division rate;
 - (b) using a delay chain in which delay units are coupled in series and delaying said input signal by selecting a number of said delay units to output said output signal;
 - (c) dividing a frequency of said output signal by a second division rate higher than said first division rate;
 - (d) delaying a signal obtained by said step (c) by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer;
 - (e) comparing phases of signals obtained by said steps (a) and (d);
- and
- (f) selecting the number of said delay units in response to a comparison result in said step (e).

10. (Currently Amended) A delay time adjusting method for receiving a signal that is input to an input buffer, as an input signal via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal, comprising the steps of:

(a) using a delay chain in which delay units are coupled in series and delaying said input signal by selecting a number of said delay units to output said output signal;

(b) dividing a frequency of said output signal by a division rate, wherein a frequency of a signal obtained by said step (b) is less than a frequency of said input signal;

(c) delaying the signal obtained by said step (b) by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer;

(d) comparing phases of said input signal and the signal obtained by said step (c); and

(e) selecting the number of said delay units in response to a comparison result in said step (d).

11. (Previously presented) The delay time adjusting method as claimed in claim 9, wherein said step (e) supplies a signal indicating said comparison result to said step (f) according to said signal generated by said step (c) and obtained via said step (d).